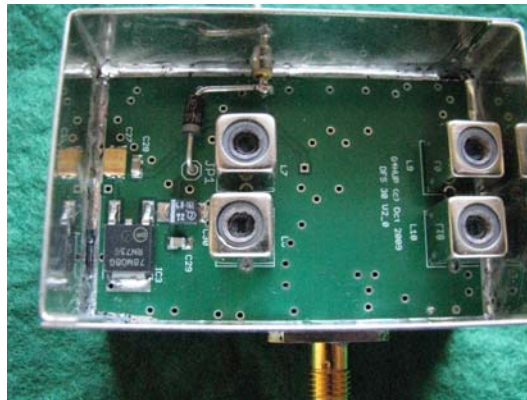


# G4HUP

## DFS30 GPS Lock for IC706/746 Series Transceivers

### Technical Manual



Document Author  
Date  
Version  
Document Ref

Dave Powis, G4HUP  
2 Dec 2009  
Issue 2.01  
HUP-05-021

## Contents

|   |          |
|---|----------|
| <b>Unit Specifications</b> .....            | <b>3</b> |
| <b><i>Scope of Document</i></b> .....       | <b>4</b> |
| <b>Physical Description</b> .....           | <b>4</b> |
| <b>DFS30 Operation Overview</b> .....       | <b>4</b> |
| <b>Circuit Description</b> .....            | <b>5</b> |
| Input Buffer Circuit – Fig 2.....           | 5        |
| Diode Multiplier – Fig 2.....               | 6        |
| Band Pass and Low Pass Filters – Fig 3..... | 6        |
| Voltage Regulator – Fig 3 .....             | 6        |
| <b><i>Construction</i></b> .....            | <b>6</b> |
| <b><i>Setting Up</i></b> .....              | <b>7</b> |
| <b>Connection to IC706</b> .....            | <b>7</b> |
| <b>Errata and Addenda</b> .....             | <b>7</b> |
| <b>Component Locations</b> .....            | <b>7</b> |
| <b>Maintenance</b> .....                    | <b>7</b> |
| Construction Practices.....                 | 7        |
| <b>Change History</b> .....                 | <b>8</b> |

## Unit Specifications

Model Ref DFS30 Issue 2

Serial No

|                  |         |                                 |
|------------------|---------|---------------------------------|
| Input Frequency  | 10      | MHz                             |
| Input Level      | +10     | dBm                             |
| Output Frequency | 30      | MHz                             |
| Output Level     | +5      | dBm                             |
| Supply Voltage   | 10 – 15 | V                               |
| Supply Current   | 110     | mA @ 13vdc                      |
| Spurii           | <-65    | dBc - typical                   |
| Harmonic output  | <-60    | dBc – second harmonic - typical |

\*Note: Current shown is with input stage equipped. With no input buffer, I = 50mA.  
Output level quoted is without any attenuator in the output circuit.

## Scope of Document

This document is intended to provide all necessary information to guide users in the construction and installation of the G4HUP DFS30 in normal operation. It also applies, with some changes of component values in the tuned circuits to variants giving 50MHz, 70MHz and 90MHz outputs.

Ready built units are supplied complete and tested, and should require no further attention prior to use.

This document is relevant for DFS30 units constructed on DFS30 Issue 2 PCB's.

Reference data can be found on the Frequency Converter pages of the DFS web-site, including any identified issues or problems – <http://g4hup.com/DFS30/DFS30.html>.

## DFS30 Description

### *Physical Description*

The DFS V2.00 is constructed in a tin-plate housing, measuring 55 x 37 x 30 mm (2.2 x 1.45 x 1.2 inches approx)

External connections are provided for:

- Reference signal in – 10MHz
- Output signal – 30MHz
- +Vcc power supply
- 0v DC ground

All RF connections use SMA female panel connectors

DC connections are by solder terminations to the DC input feedthrough capacitor and the ground tag close by it.

### *DFS30 Operation Overview*

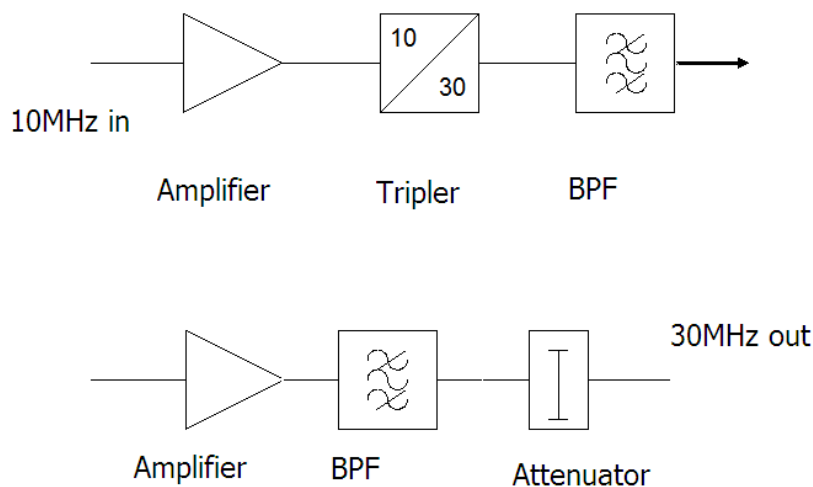
The DFS30 is designed to accept a 10MHz GPS locked input signal at a nominal +10dBm level. As an alternative to a GPS locked input signal, the output of a good quality OXCO, amplified to the correct level, can be used, with entirely satisfactory results.

The output of the unit is a 30MHz GPS locked reference signal for providing the master oscillator frequency for the Icom IC706 and 746 range of transceivers. This facilitates absolute GPS locking of the transceiver for normal operation, and when used in conjunction with microwave transverters that are themselves GPS locked, results in a high precision amateur station for any band.

Higher frequency versions of the DFS30 – ie DFS50, DFS70 and DFS90 are intended to provide LO sources for SDR down converters. The operation is essentially identical to the DFS30, the only difference being the harmonic that is selected from the diode multiplier output by the tuned circuits. There may be minor differences in output signal amplitudes, due to higher order harmonics being used.

### ***Circuit Description***

The main circuit blocks are shown in Fig 1, and are described in the following sections, which refer to the circuit diagrams at the end of this manual.



**Fig 1 – DFS30 block functions**

### **Input Buffer Circuit – Fig 2**

The input buffer circuit comprises of an attenuator followed by a MMIC buffer amplifier, with approximately 18dB of gain. Its main purpose is to provide amplification and gain adjustment where the available input signal level is below +10dBm. Where the source provides this level already, then the input buffer can be omitted. In this case strap the input connector directly through to C2 – it is recommended that C2 is retained to provide DC isolation.

Should the drive source supply more than +10dBm, then use the input attenuator to reduce the level to achieve the required +10dBm at C2.

## Diode Multiplier – Fig 2

The diode multiplier is a comb generator, and produces output components beyond 400MHz. The following filter selects the 30MHz component and reduces the levels of the others to insignificant levels.

This filter, F1, is a two stage LC filter, using capacitive top-coupling. Capacitive taps are used at input and output to match into the surrounding stages.

A single MMIC amplifier stage with approx 20dB follows the filter to amplify the signal. An attenuator is provided between the filter and the MMIC, providing adjustment to ensure the MMIC is operating in its linear range – this attenuator is not used on the Iss2 PCB and should be set to 0dB.

## Band Pass and Low Pass Filters – Fig 3

A second bandpass filter at 30MHz follows the amplifier. This is optionally followed by a low pass filter, although use of the LPF is not necessary in this application.

Finally, there is an attenuator to allow the output level to be defined. The attenuator value should be set to give an output of between +5dBm and +10dBm to drive the IC706 correctly. The attenuator is not normally required, so make sure that R203 is replaced by a short circuit bridge.

## Voltage Regulator – Fig 3

Only an 8v rail is required in this application, so there is a single D-PAK type 0.5A regulator installed as IC3.

Not shown on the diagram is the 1nF feedthrough capacitor, C31, which is used to bring the nominal +12v DC into the circuit enclosure, with diode D2 in series.

## Construction

Due to the compact nature of the DFS30 Iss2, there is a recommended order of construction. Some parts will be difficult to install if the sequence is not followed.

- 1 Mark and drill the box sides – de-burr and solder the two halves together. Mount the two SMA connectors onto the box sides
- 2 Trim the PCB to fit in the box, so that it rests on the two connector spills.
- 3 Assemble all the components onto the PCB, with the exception of the regulator, IC3, capacitor C27 and the four 1uH 7KLL inductors, L6, L7, L9 and L10.
- 4 Mount the PCB into the box, soldering the two connector spills to the tracks, and then seam solder the PCB to the box all round, top and bottom.
- 5 Install the regulator IC3 and C27

- 6 Install the 1uH inductors
- 7 Install the feed through capacitor, with its solder tag, and the diode D1

## Setting Up

After a visual check of the construction, connect the supply and measure the current drawn at 13.8v – it should be  $110 \pm 10\text{mA}$ . Confirm that the voltage at the regulator output is  $8 \pm 0.2\text{v}$ , and that the DC supply voltage present at the pin of IC1 and IC2 is close to 4.3 and 3.6v respectively. This completes the DC tests.

Connect a 10MHz source at +10dBm, to the input and a spectrum analyzer to the output. You should already see a low level response at 30MHz. Peak coils L6 and 7 to maximize the multiplier output, followed by L9 and 10 to peak the amplifier output – the final level achieved should be  $5 \pm 2\text{dBm}$ .

Check that the second harmonic is at  $-60\text{dBc} \pm 2\text{dBm}$

### **Connection to IC706**

See <http://g4hup.com/mods/html> for details on performing the conversion.

### **Errata and Addenda**

This section contains information about components that have been changed or added compared with the original PCB design.

See <http://g4hup.com/DFS/DFSerrata.html> for full details, versions impacted and resolution guidance, including pictorial support.

### **Component Locations**

Figs 4 and 5 respectively show the locations of components on the top side and lower side of the PCB

Fig 6 shows a spectrum analyzer trace of the output signal over the range 5 to 95MHz

### **Maintenance**

#### **Construction Practices**

Ready built units are assembled using lead bearing solder - any repairs or changes necessary should be made using lead based solder. Use as small a grade of good quality flux based electronic assembly solder as possible.

Kits are not supplied with any solder, but it is recommended that a small diameter, good quality cored flux solder is used, to ensure minimum flux residues on the PCB

after assembly. The PCB will accept lead-free solder, and components used are generally ROHS compliant, and should therefore also accept lead-free solder if you prefer.

It is recommended that lead based solder is used for maximum reliability of soldered joints.

### Change History

| <b>Date</b> | <b>Iss No</b> | <b>Comment</b>                  | <b>Author</b> |
|-------------|---------------|---------------------------------|---------------|
| 7 Jul 08    | 1.0           | First version                   | G4HUP         |
| 20 Nov 09   | 2.0           | Iss 2 – updated for Iss 2 PCB's | G4HUP         |
| 2 Dec 09    | 2.01          | Minor documentation corrections | G4HUP         |
|             |               |                                 |               |
|             |               |                                 |               |
|             |               |                                 |               |
|             |               |                                 |               |

End of text – Diagrams follow

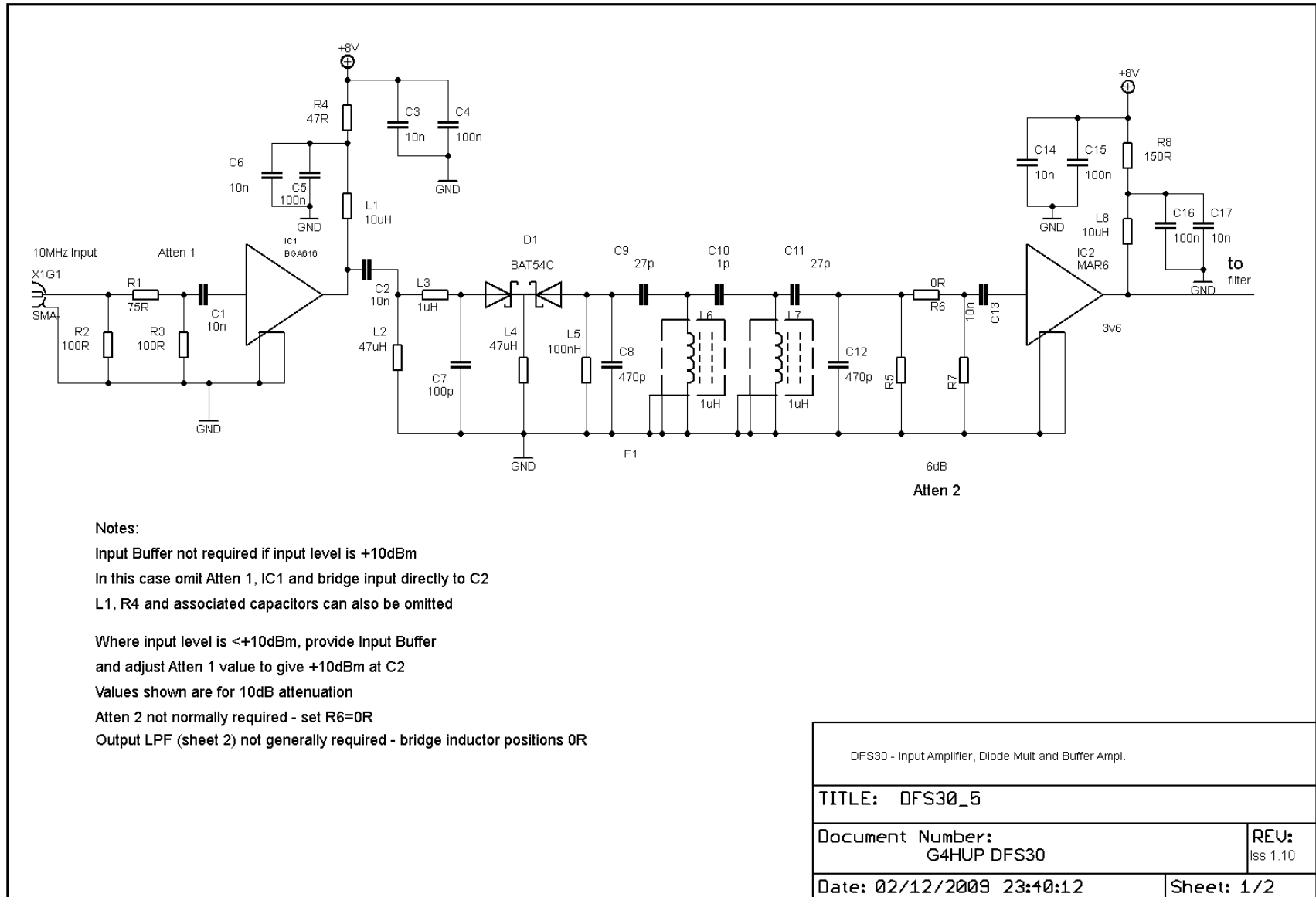


Fig 2 – Input Amplifier, Diode Multiplier and Buffer Amplifier circuit

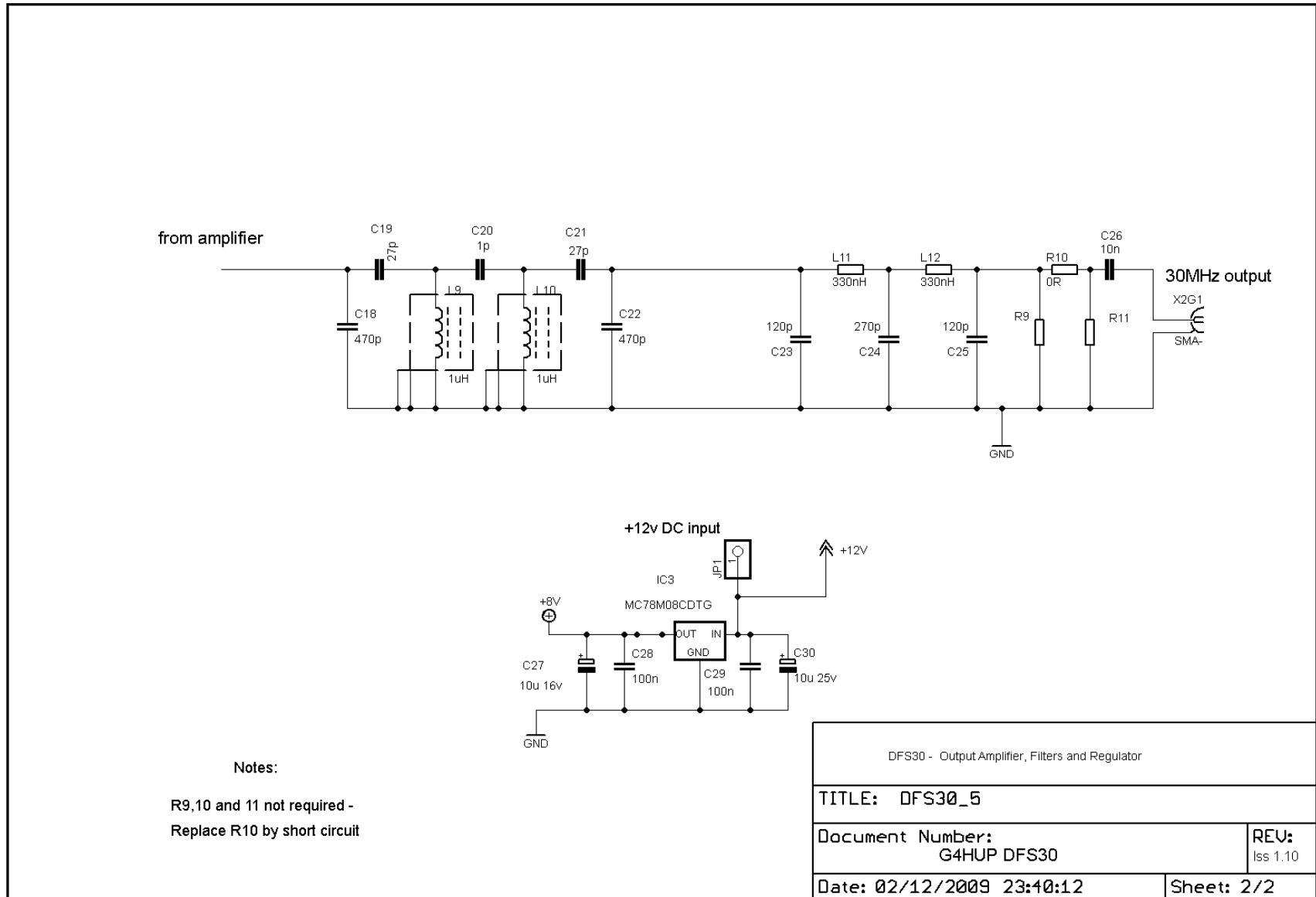


Fig 3 – Output Filters and Voltage Regulators

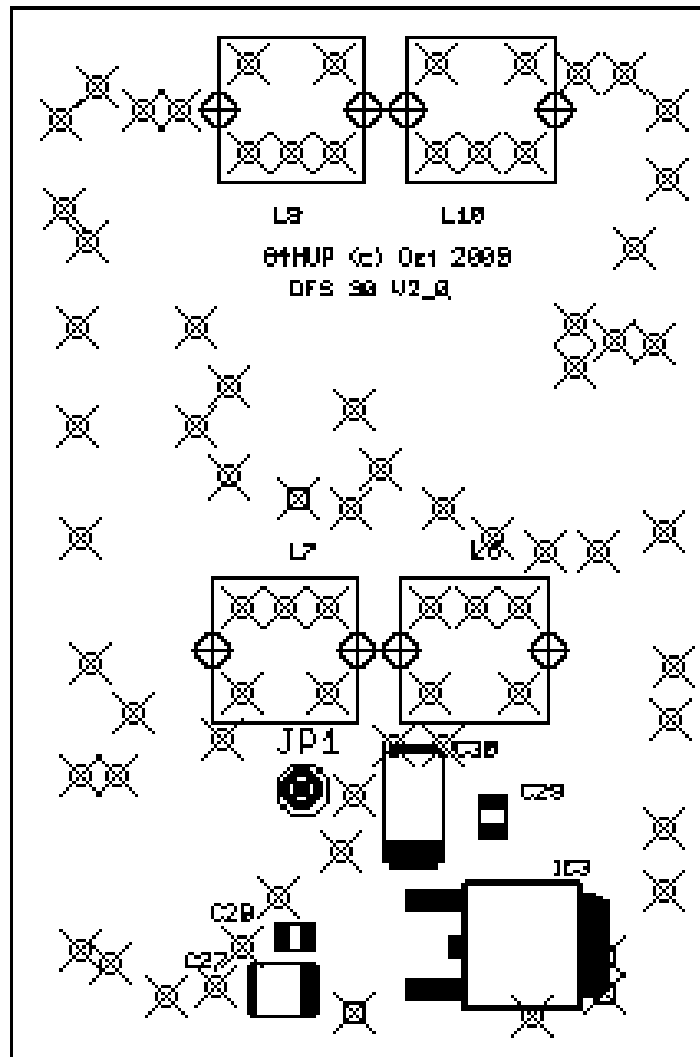


Fig 4 – Top side PCB overlay

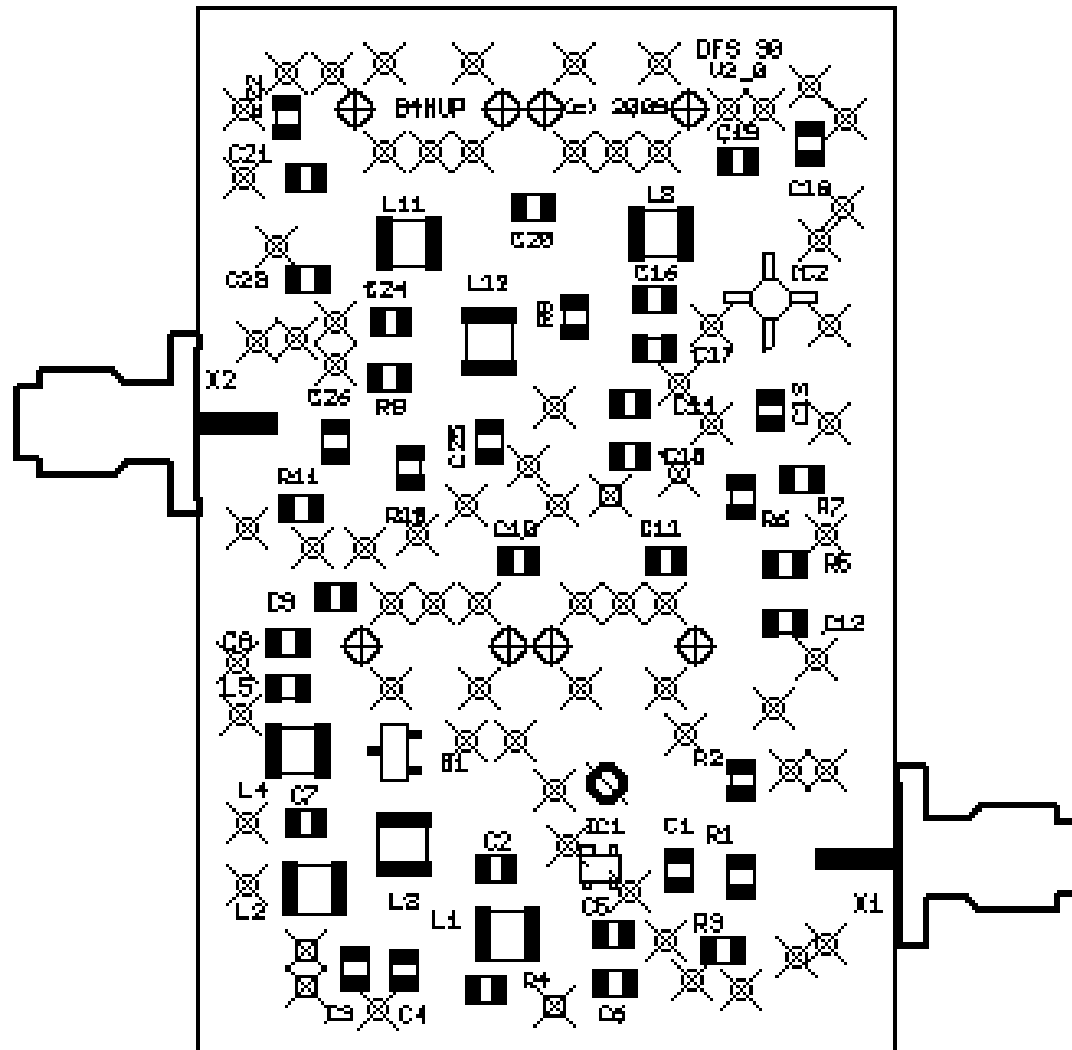
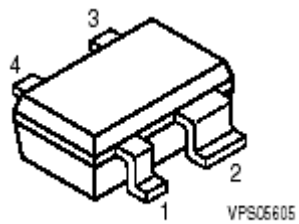
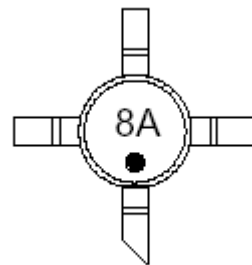


Fig 5 – Underside PCB Component Overlay



BGA616 1 – i/p, 3 – o/p



MAR-6 – dot is input

Fig 6 – Component orientation diagrams